CLAIMS

What is claimed is.

1. A polymer memory device comprising:

a series of first electrodes;

an array of discrete, spaced-apart polymer structures disposed over the series of first electrodes; and

a series of second electrodes disposed over the discrete, spaced-apart polymer structures.

2. The polymer memory device according to claim 1, wherein the first electrodes have a first width, wherein the second electrodes have a second width, and wherein a given polymer structure in the array of discrete, spaced-apart polymer structures has an area that is greater than the product of the first width and the second width.

3. The polymer memory device according to claim 1, wherein the first and second electrodes have a width that is a minimum feature of a photolithography technology selected from 0.25 micron, 0.18 micron, 0.13 micron, and 0.11 micron.

4. The polymer memory device according to claim 1, further comprising:

a protective film disposed above and on the electrodes.

5. The polymer memory device according to claim 1, further comprising:

an organic protective film disposed above and on the electrodes.

6. The polymer memory device according to claim 1, wherein each electrode in the series of electrodes has four rectilinear surfaces in cross-section, and wherein each electrode in the series of first electrodes is contacted by the ferroelectric polymer structure on three of the four surfaces.

7. The polymer memory device according to claim 1, wherein the series of first electrodes comprises a damascene structure disposed in a substrate.

8. The polymer memory device according to claim 1, wherein the array of discrete, spaced-apart polymer structures further comprise a polymer selected from $(CH_2\text{-}CF_2)_n$, $(CHF\text{-}CF_2)_n$, $(CF_2\text{-}CF_2)_n$, α-, β-, γ-, and δ-phases thereof, $(CH_2\text{-}CF_2)_n\text{-}(CHF\text{-}CF_2)_m$ copolymer, α-, β-, γ-, and δ-phases thereof, and combinations thereof.

9. A process of forming a polymer memory structure comprising:

first patterning a ferroelectric polymer structure to match a first electrode layout; and

second patterning the ferroelectric polymer structure to match a second electrode layout.

10. The process according to claim 9, wherein first patterning further comprises:

patterning the ferroelectric polymer structure over the first electrode layout under conditions that substantially cover the first electrode layout and that forms segmented, elongated ferroelectric polymer structures.

11. The process according to claim 9, wherein second patterning further comprises:

patterning the segmented, elongated ferroelectric polymer structures by using the second electrode layout as an etch mask.

12. The process according to claim 9, before first patterning a ferroelectric polymer structure according to a first electrode layout, the process further comprising:

providing a substrate; and

forming the first electrode layout as a damascene structure in a substrate.

13. The process according to claim 12, after second patterning a ferroelectric polymer structure according to a second electrode layout, the process further comprising:

forming an organic protective film above and on electrode layouts.

14. The process according to claim 9, before first patterning a ferroelectric polymer structure according to a first electrode layout, the process further comprising:

providing a substrate;

forming the first electrode layout upon an upper surface of the substrate.

15. The process according to claim 14, after second patterning a ferroelectric polymer structure according to a second electrode layout, the process further comprising:

forming an organic protective film above and on electrode layouts.

16. A process of forming a memory device comprising:

providing a ferroelectric polymer structure between an array of intersecting lower and upper electrodes; and

removing ferroelectric polymer material that is laterally exposed between the array of electrodes.

17. The process according to claim 16, wherein providing a ferroelectric polymer structure between an array of intersecting lower and upper electrodes further comprises:

providing a substrate;

forming the lower electrode layout;

forming the ferroelectric polymer structure over the lower electrode layout;

first patterning the ferroelectric polymer structure to form segmented, elongated ferroelectric polymer structures; and

forming the upper electrode layout.

18. The process according to claim 17, wherein removing ferroelectric polymer material that is laterally exposed between the array of electrodes further comprises:

first patterning the ferroelectric polymer structure to form segmented, elongated ferroelectric polymer structures; and

second patterning the ferroelectric polymer structure to form discrete, spaced-apart ferroelectric polymer structures.

19. The process according to claim 18, wherein second patterning further comprises:

patterning the segmented, elongated ferroelectric polymer structures by using the upper electrode layout as an etch mask.

20. The process according to claim 17, before first patterning, the process further comprising:

providing a substrate; and

forming the lower electrode layout as a damascene structure in the substrate.

21. The process according to claim 18, after second patterning, the process further comprising:

forming an organic protective film above and on electrode layouts.

22. The process according to claim 17, before first patterning, the process further comprising:

providing a substrate; and

forming the lower electrode layout upon an upper surface of the substrate.

23. The process according to claim 22, after second patterning, the process further comprising:

forming an organic protective film above and on electrode layouts.

24. A memory system comprising:

a substrate disposed on a physical interface for a host;

a memory article disposed on the substrate, the memory article comprising:

a series of first electrodes;

an array of discrete, spaced-apart polymer structures disposed over the series of first electrodes; and

a series of second electrodes disposed over the discrete, spaced-apart polymer structures; and

a signal interface for communication from the memory article to the host; and

a host.

25. The memory system according to claim 24, wherein the physical interface is configured to a host interface that is selected from a PCMCIA card interface, a compact flash card interface, a memory stick-type card interface, a desktop personal computer expansion slot interface, and a removable medium interface.

26. The memory system according to claim 24, wherein the first and second electrodes have a width that is a minimum feature of a photolithography technology selected from 0.25 micron, 0.18 micron, 0.13 micron, and 0.11 micron.

27. The memory system according to claim 24, further comprising:
a protective film disposed above and on the electrodes.

28. The memory system according to claim 24, wherein the series of first electrodes is contacted by the ferroelectric polymer structure on three of four surfaces.

29. The memory system according to claim 24, wherein the series of first electrodes comprises a damascene structure disposed in a substrate.